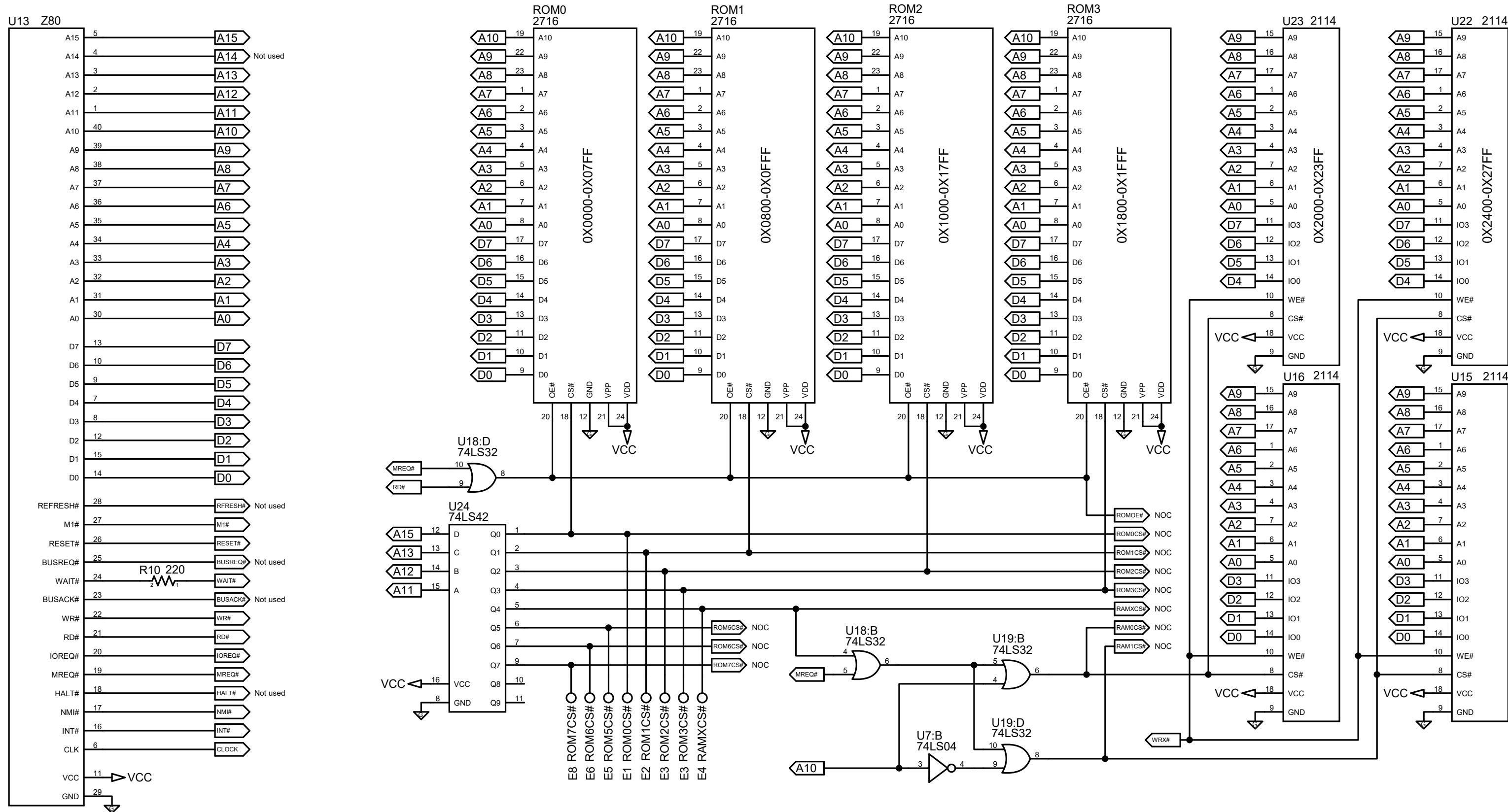
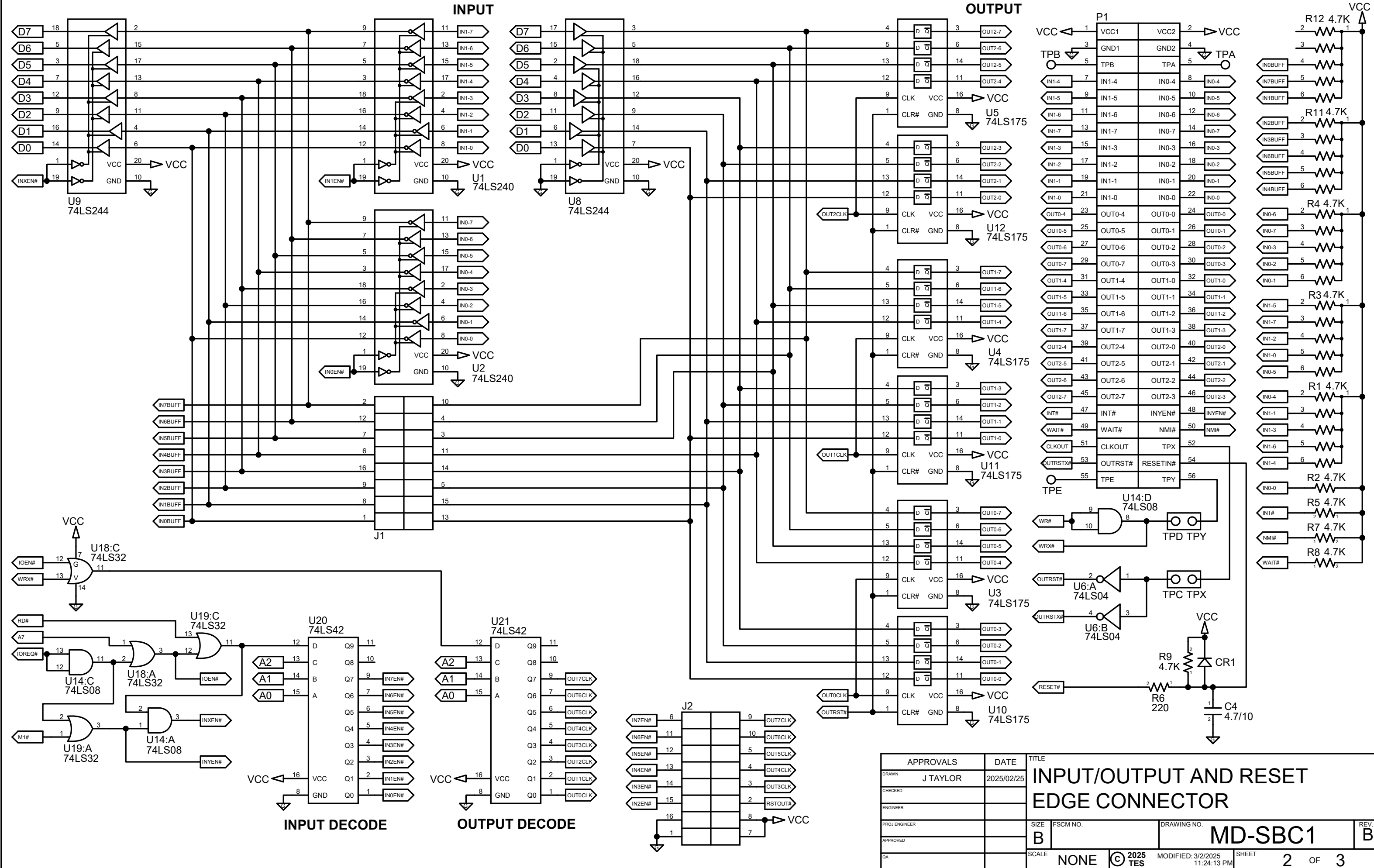


REVISION HISTORY		APPROVED	DATE
REV	DESCRIPTION	J Taylor	2025/02/25
B	Initial release		

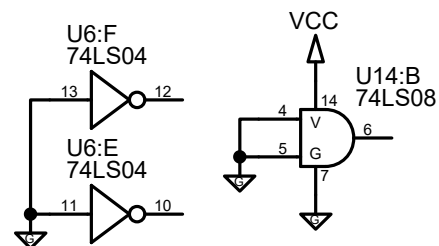
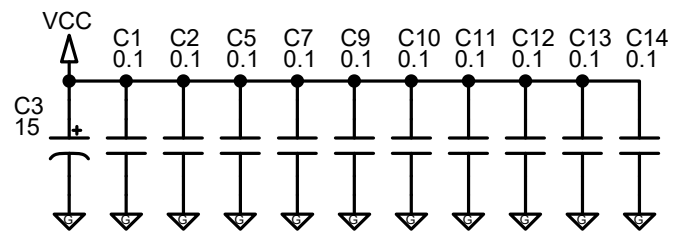
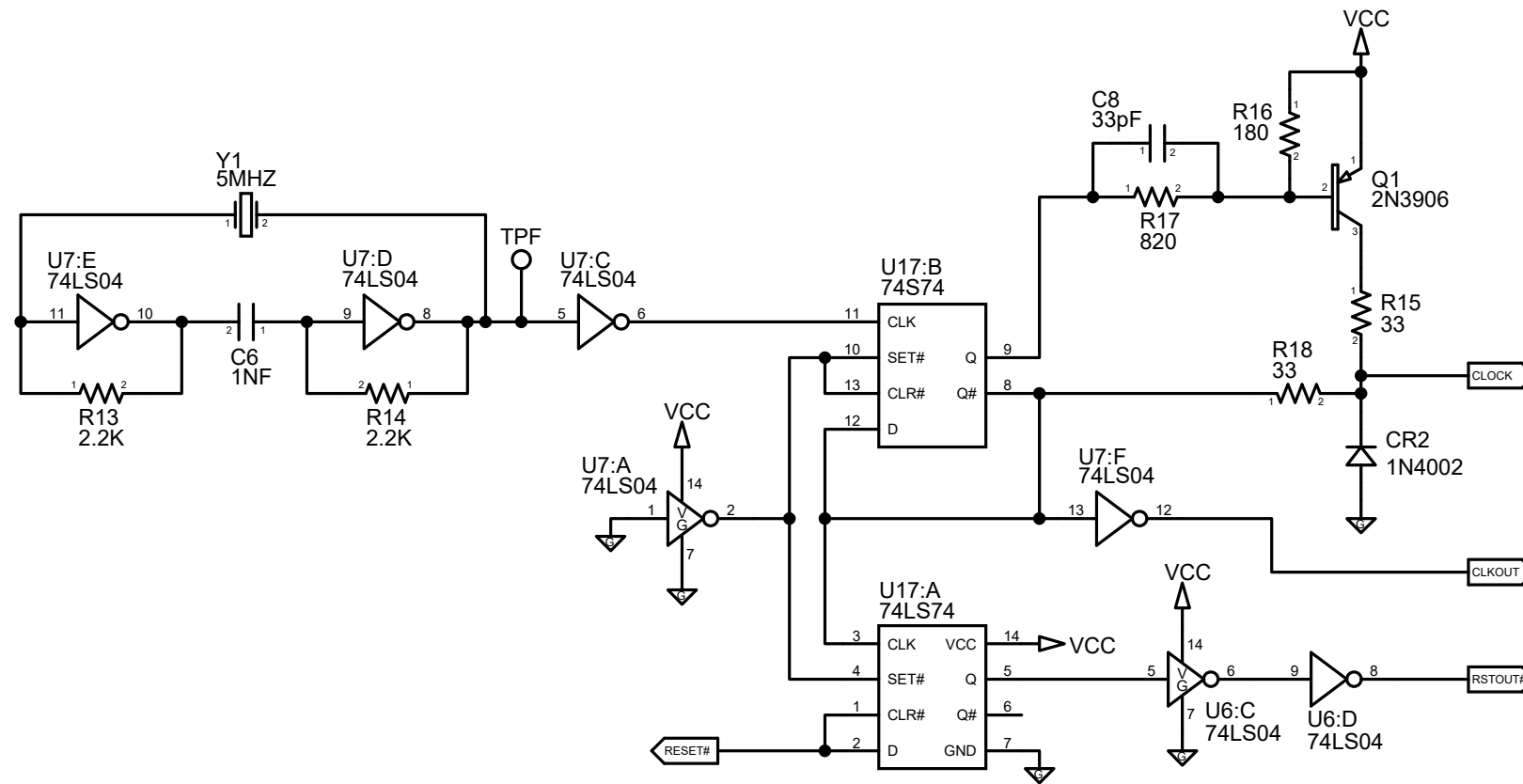


APPROVALS		DATE	TITLE			
DRAWN	J TAYLOR	2025/02/25	CPU / ROM AND RAM DECODE			
CHECKED						
ENGINEER						
PROJ ENGINEER						
APPROVED			SIZE	FSCM NO.	DRAWING NO.	REV
GA			B		MD-SBC1	B
SCALE		NONE	© 2025 TES	MODIFIED: 3/2/2025 11:24:13 PM	SHEET	1 OF 3

NOTES: UNLESS OTHERWISE SPECIFIED



APPROVALS		DATE	TITLE		
DRAWN	J TAYLOR	2025/02/25	INPUT/OUTPUT AND RESET EDGE CONNECTOR		
CHECKED					
ENGINEER					
PROJ ENGINEER			SIZE	FSCM NO.	DRAWING NO.
APPROVED			B		MD-SBC1
GA			SCALE	NONE	REV B
			© 2025 TES	MODIFIED: 3/2/2025 11:24:13 PM	SHEET 2 OF 3



APPROVALS		DATE	TITLE		
DRAWN	J TAYLOR	2025/02/25	CLOCK GENERATION SPARES AND DECOUPLING		
CHECKED					
ENGINEER					
PROJ ENGINEER			SIZE	FSCM NO.	DRAWING NO.
APPROVED			B		MD-SBC1
QA			SCALE	© 2025 TES	MODIFIED: 3/2/2025 11:24:13 PM
			NONE	SHEET	3 OF 3
					REV. B